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09/347,409	07/06/1999	TETSUYA AKIMOTO	Q55026	3821

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EXAMINER
DAY, HERNG-DER

ART UNIT	PAPER NUMBER
2123	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/347,409	Applicant(s) AKIMOTO ET AL.	
	Examiner Herng-der Day	Art Unit 2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July1999* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) ____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 August 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to Applicant's Reply to Office Action dated June 7, 2002, mailed on August 27, 2002.

1-1. Claims 1-12 were amended; claims 1-12 are pending.

1-2. Claims 1-12 have been examined and claims 1-12 have been rejected.

Information Disclosure Statement

2. Regarding the Japanese Office Action, the Examiner has obtained a full translation of the Japanese Office Action dated July 12, 2000, which is titled "REASON FOR REJECTION". This translation will be provided to the Applicant through form PTO-892, Notice of References Cited. Therefore, the Examiner has considered this Japanese Office Action, and has amended form PTO-1449, Information Disclosure Statement(s), to document this consideration. A copy of the amended form PTO-1449 will be provided to the Applicants.

Drawings

3. Regarding drawings, the proposed drawing correction of Fig.1 is approved. However, the submitted "proposed correction of Fig. 3", as mentioned in the third paragraph, page 11 of the Applicants' Reply, has not been received. Also note, the corrected drawings in response to form PTO-948, Notice of Draftsperson's Patent Drawing Review, will be submitted, as mentioned in the second paragraph, page 12 of the Applicants' Reply, has not been received yet.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The Examiner has acknowledged without objection that the title has been amended.

5. Regarding the specification, several amended paragraphs of the specification are approved. However, the submitted "proposed correction of Fig. 3", as mentioned in the third paragraph, page 11 of the Applicants' Reply, has not been received. Therefore, the specification of "the delay time degradation rate calculation 305" in line 12 of page 12 is still objected. Appropriate correction is required.

Claim Objections

6. The Examiner has acknowledged without objection that claim 4 has been corrected.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 3 and 5 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

For example, as described from the last line of page 12 to line 4 of page 13, the delay time calculation 402 is a conventional method for calculating pin-to-pin delay time and block-to-block delay time without reference to the hot electron effect. The amended claim 3 recites the limitation "(a) calculating the pin-to-pin delay time, based on a value V_C of a transistor property of a transistor included in the logic block, and the block-to-block delay time without calculating in aging caused by hot carrier effect". However, the new subject matter "based on a value V_C of a transistor property of a transistor included in the logic block" was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 5 is rejected as being dependent on the rejected claim 3.

9. Claims 3-6 and 9-12 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

For example, as described in lines 2-4 of page 4 and in lines 15-17 of page 6, the block-to-block delay time $T_{connect\_aged}$ is delay time of a signal passing between said two logic blocks connected to each other by a computer. However, it is unclear for one skilled in the art why two logic blocks are not connected to each other by only wire(s) or conductor(s) but by a computer. Accordingly, it is unclear how one skilled in the art may make and/or use the invention by calculating the block-to-block aged signal delay time $T_{connect\_aged}$ of two logic blocks connected

to each other by a computer because the calculation of the delay time introduced by the computer has not been disclosed in the specification.

Next, as described in page 19, a logic block comprising three stage inverters each of which has the same delay time. When the input changes from low level to high level, λ is shown by expression (31) and when the input changes from high level to low level, λ is shown by expression (32). Based on expression (32), the delay time for input changes from high level to low level will be zero. Accordingly, it is unclear for one skilled in the art why the value of λ in expression (31) is not 1 / 2 because in the middle stage the input changes from high level to low level. Similarly, it is unclear for one skilled in the art about expressions (33) and (34) for four stage inverters.

Therefore, claims 3-4 and 9-10 eventually contain subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 5-6 and 11-12 are rejected because they are dependent on rejected claims.

10. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 7-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11-1. Claim 7 recites the limitation "the product" in line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "the product" as described in claim 7 refers to "the program".

11-2. Claim 8 is rejected as being dependent on the rejected claim 7.

11-3. Claim 9 recites the limitation "the product" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "the product" as described in claim 9 refers to "the program".

11-4. Claim 10 recites the limitation "the product" in line 5 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "the product" as described in claim 10 refers to "the program".

11-5. Claim 11 recites the limitation "the product" in line 3 and line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "the product" as described in claim 11 refers to "the program".

11-6. Claim 12 recites the limitation "the product" in line 3 and line 4 of the claim. There is insufficient antecedent basis for this limitation in the claim. For the purpose of claim examination, the Examiner will presume that "the product" as described in claim 12 refers to "the program".

Claim Rejections - 35 USC § 101

12. The Applicants have amended all the claims and the requirements of 35 U.S.C. 101 are met. Therefore, the claim rejections of claims 1-12 under 35 U.S.C. 101 have been withdrawn.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

14. Claims 9 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Iwanishi et al., U.S. Patent 6,047,247 issued April 4, 2000, and filed December 5, 1997.

14-1. Regarding claim 9, Iwanishi et al. disclose a computer-readable medium incorporating a program of instructions for calculating a delay time of a signal passing through a logic level circuit which consists of a plurality of logic blocks from pin-to-pin delay time, which is delay time of a signal passing between an input pin and an output pin of a logic block, and block-to-block delay time, which is delay time of a signal passing between two logic blocks connected to each other, the program making a computer execute the following processes:

(a) calculating the pin-to-pin delay time and the block-to-block delay time without calculating in aging caused by hot carrier effect (delay calculation step, column 4, lines 53-63);

(b) calculating variations of delay times that signals pass through transistors connected to the input and output pin caused by said aging (delay degradation amount calculation step, column 4, line 63 to column 5, line 9); and,

(c) modifying the pin-to-pin delay time and the block-to-block delay time calculated in step (a) by the variations calculated in step (b), and outputting said modified values for use as values representative of circuit properties of said logic level circuit (after-deterioration delay calculation step, column 5, lines 9-13).

14-2. Regarding claim 11, Iwanishi et al. disclose that the program making a computer execute the following processes:

(a) calculating delay times of all said logic blocks according to the product as in claim 9 (delay calculation step, delay degradation amount calculation step, and after-deterioration delay calculation step, column 4, line 53 to column 5, line 13); and,

(b) calculating and outputting for use as a value representative of a circuit property of said logic level circuit the delay time of the logic level circuit from the result of step (a) (deterioration is estimated, column 5, lines 13-16).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 1-2 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwanishi et al., U.S. Patent 6,047,247 issued April 4, 2000, and filed December 5, 1997, in view of Fang et al., U.S. Patent 6,278,964 issued August 21, 2001 and filed May 29, 1998.

16-1. Regarding claim 1, Iwanishi et al. disclose a method of calculating, by the use of a computer, a numerical value V_A representative of a circuit property of a logic level circuit, from a numerical value V_B, which shows a block property of a logic block included in the logic level circuit, comprising the steps of:

(a) calculating the V_B (delays of the cells, delays of the cell-to-cell wirings, column 6, lines 39-40) from a plurality of numerical values V_C (circuit information of the LSI, column 6, line 37), each value V_C representing a transistor property of a transistor included in the logic block; and,

(b) calculating the V_A from the V_B, and outputting V_A for use as a value representative of a circuit property of said logic level circuit (delay calculation of an LSI, column 6, lines 35-36).

However, Iwanishi et al. do not expressly disclose that each value V_C representing a transistor property of a transistor included in the logic block. Nevertheless, Iwanishi et al. do suggest that the calculation of V_B based on circuit information.

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line

12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 1 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

16-2. Regarding claim 2, following the same analysis as in section **16-1** for claim 1, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices. Accordingly, V_Cs (device parameters) of a transistor (device) connected to an input pin of a logic block and V_Cs of a transistor connected to an output pin of a logic block, among other V_Cs, definitely will be provided to simulate device performance and to determine voltages and currents at each node within the cells (Fang, column 6, line 66 through column 7, line 4).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 2 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

16-3. Regarding claim 7, Iwanishi et al. disclose a computer-readable medium incorporating a program of instructions for calculating a numerical value V_A, which shows a property of a logic

level circuit, from a numerical value V_B, which shows a property of a logic block constituting the logic level circuit, the program making a computer execute the following processes:

(a) calculating the V_B (delays of the cells, delays of the cell-to-cell wirings, column 6, lines 39-40) from a plurality of numerical value V_C (circuit information of the LSI, column 6, line 37), each V_C showing a property of a transistor constituting part of the logic block; and,

(b) calculating the V_A from the V_B, and outputting V_A for use as a value representative of a circuit property of said logic level circuit (delay calculation of an LSI, column 6, lines 35-36).

However, Iwanishi et al. do not expressly disclose that each value V_C representing a transistor property of a transistor included in the logic block. Nevertheless, Iwanishi et al. do suggest that the calculation of V_B based on circuit information.

Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). In other words, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 7 because Fang et al. disclose in detail the

circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

16-4. Regarding claim 8, following the same analysis as in section **16-3** for claim 7, Fang et al. disclose that the circuit information needed for simulating the hot-carrier effects includes a set of device (transistor) parameters (property of a transistor) for all devices. Accordingly, V_Cs (device parameters) of a transistor (device) connected to an input pin of a logic block and V_Cs of a transistor connected to an output pin of a logic block, among other V_Cs, definitely will be provided to simulate device performance and to determine voltages and currents at each node within the cells (Fang, column 6, line 66 through column 7, line 4).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Iwanishi et al. to incorporate the teachings of Fang et al. to obtain the invention as specified in claim 8 because Fang et al. disclose in detail the circuit information, which will be the input for simulating the hot-carrier effects, as suggested by Iwanishi et al.

Allowable Subject Matter

17. The equations of claims 4, 6, 10, and 12 are not taught exactly by the prior art, and would be allowable if the above rejections under 35 U.S.C. 112, first and second paragraphs are overcome.

Applicant's Arguments

18. Applicants argue that the rejections made under 35 U.S.C. 102(e) for claims 1-3,5,7-9, and 11 are inapplicable because:

(1). Iwanishi does not disclose or suggest using V_C for calculating V_C (Reply, page 14, lines 4-5).

(2). Iwanishi does not disclose or suggest using for calculation V_C, a transistor property of a transistor included in the transistor block (Reply, page 14, lines 3-4 and 17-18; page 15, lines 6-7; page 16, lines 5-6). The claimed invention requires calculating the V_B from numerical values V_C (Reply, page 13, lines 13-14).

(3). Iwanishi does not disclose or suggest that the circuit information 11, the delay library 12, or the input slew calculated therefrom relate to a transistor property, V_C (Reply, page 15, lines 14-16).

(4). Iwanishi does not disclose or suggest that the circuit information 11, the delay library 12, or the output load capacitance calculated therefrom relate to a transistor property, V_C (Reply, page 16, lines 2-3).

Response to Arguments

19. Applicants' arguments have been fully considered. They are not persuasive except for argument (1).

19-1. Response to Applicants' arguments (2)-(4). The Applicants argue that Iwanishi does not disclose or suggest using V_C, a transistor property of a transistor included in the transistor block, for calculation V_B, a block property of a logic block.

Iwanishi discloses a hot carrier-delay-degradation estimation method comprises a delay calculation step of calculating delays, signal waveform inclinations at the input terminals, and load capacitances connected to the output terminals based on circuit information 11 and a delay library. The circuit information comprises characteristic information of the cell and other information (column 2, lines 50-65).

It is well known for one skilled in the art that a plurality of numerical values, V_Cs, and a plurality of calculated V_Bs, are provided from the circuit information to support the delay calculation step. As an example, in the cited reference, Fang et al. disclose a detailed description of the IC cell data 102, which specifies characteristics and properties of the cells in the IC that are to be included in the simulation for hot-carrier effects (Fang, column 5, lines 38-45). IC cell data 102 includes the device model data to determine voltages and currents at each node within the cells. The device model data includes time-based mathematical models that typically include a set of device parameters and a set of complex equations which must be solved to simulate device performance (Fang, column 6, line 12 through column 7, line 39). Accordingly, V_Cs (device parameters) of a transistor (device) connected to an input pin of a logic block and V_Cs of a transistor connected to an output pin of a logic block, among other V_Cs, definitely will be provided to simulate device performance and to determine voltages and currents at each node within the cells.

Fang et al. also disclose that most commercially available circuit simulation packages provide default device parameters and models which can be modified to suit a particular fabrication process or application (Fang, column 7, lines 4-12), therefore, users are not required

to start from scratch. Accordingly, Fang et al. even suggest that the limitation (a) in claim 1 and 7 has been met in most commercially available circuit simulation packages.

After all, even Iwanishi does not expressly disclose or suggest that the circuit information includes V_C, however, when combined with the disclosure of Fang et al., or by the disclosure of Fang et al. alone, calculating the V_B from numerical values V_C has been taught.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference to the translated copy of "REASON FOR REJECTION", Japanese Office Action dated July 12, 2000, is cited with explanation in section **2** above.

21. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

22. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
December 10, 2002

KEVIN J. TESKA
SUPERVISORY
PATENT EXAMINER